Amendments to the Specification:

Amend the specification by inserting a new section before the "Technical Field" as follows:

-- CROSS-REFERENCE TO RELATED APPLICATION

This application is a divisional of pending United States Patent Application No. 10/074,176, filed February 11, 2002. --

Please amend the paragraph at page 1, line 17-page 2, line 2, as follows:

A typical flash memory comprises a memory-cell array having an array of memory cells arranged in rows and columns and grouped into blocks. Figure 1 illustrates a conventional flash memory cell 100 formed by a field effect transistor including a source 102 and drain 104 formed in a substrate 106, with a channel 108 being defined between the source and drain. Each of the memory cells 100 further includes a control gate 110 and a floating gate 112 formed over the channel 108 and isolated from the channel and from each other by isolation layers 114. In the memory-cell array, each memory cell 100 in a given row has its control gate 110 coupled to a corresponding word line WL and each memory cell in a given column has its drain 104 coupled to a corresponding bit line BL. An alternating source AS that switches between ground and an erase voltage is coupled to the source 102. The sources 102 of each memory cell 100 in a given block are coupled together to allow all cells in the block to be simultaneously erased, as will be appreciated by those skilled in the art.

Please amend the paragraph at page 3, lines 3-14, as follows:

Certain circuits within the flash memory continue operating during the standby mode to enable the flash memory to more quickly return to the active mode of operation. For example, as illustrated in Figure 2, a conventional flash memory includes a charge pump 200 that generates a word line drive voltage VX that is used by row drivers 202 in activating corresponding word lines WL. Each row driver 202 is coupled to a respective word line WL1-WLN in the memory-cell array (not shown) and receives a corresponding decoded row address signal DRA1-DRAN. When the DRA1-DRAN signal indicates the corresponding row of

memory cells 100 is to be activated, the row driver 202 applies the voltage VX to the word line WL1-WLN to thereby activate the row of memory cells 100 (not shown in Figure 2) coupled to the word line. When the DRA1-DRAN signal indicates the corresponding row of memory cells 100 is to be deactivated, the row driver 202 drives the corresponding word line WL1-WLN to ground to deactivate the row of memory cells 100.

Please amend the paragraphs at page 5, lines 23-27, as follows:

Figure 3A is a functional block diagram illustrating a voltage reference switching circuit including dual bandgap voltage references according to one embodiment of the present invention. Figure 3B is a timing diagram illustrating various signals generated during operation of the voltage reference switch of Figure 3A.

Figure 4 is a functional block diagram of a flash memory including the voltage reference switching circuit of Figure 3A.

Please amend the paragraph at page 6, lines 4-15, as follows:

Figure 3A is a functional block diagram illustrating a voltage reference switching circuit 300 including an active bandgap voltage reference 302 for generating a bandgap reference voltage VBG during an active mode of operation of a flash memory (not shown) containing the switching circuit, and including a standby bandgap voltage reference 304 for generating the bandgap reference voltage during a standby mode of operation of the flash memory, as will be explained in more detail below. The active bandgap voltage reference 302 consumes a relatively large amount of power and operates only during the active mode, while the standby bandgap voltage reference 304 consumes a relatively small amount of power and operates during the standby mode. The switching circuit 300 reduces the power consumption of the flash memory during the standby mode, and also reduces a transition time of the flash memory in switching between the active and standby modes, as will described in more detail below.

Please amend the paragraph at page 6, line 21-page 7, line 10, as follows:

The bandgap switching circuit 300 further includes a charge pump 306 that supplies a word line drive voltage VX to a plurality of row drivers 308. The charge pump 306 and row drivers 308 operate in the same manner as the charge pump 200 and row drivers 202 of Figure 2, and thus, for the sake of brevity, the operation of these components will not again be described in detail. In the bandgap switching circuit 300, a multiplexer 310 receives a first bandgap voltage VBG1 from the active bandgap voltage reference 302 and receives a second bandgap voltage reference VBG2 from the standby bandgap voltage reference 304. The multiplexer 310 applies either the VBG1 or VBG2 voltage to the charge pump 306 as the VBG voltage in response to a band gap selection signal SELBG generated by a delay circuit 312, which generates the SELBG signal in response to an internal chip enable signal CEI#. In operation, when the CEI# signal goes active low, the delay circuit 312 drives the SELBG signal low after a time delay TD. When the CEI# signal goes in active high, the delay circuit 312 drives the SELBG signal high with a substantially no time delay. With reference to Figure 3B, at a time T0, the CEI# signal goes active low, causing the SELBG signal to go low at a time T1 after the time delay TD has elapsed. At a time T2, the CEI# signal goes inactive high, and the SELBG goes high with substantially no time delay. The delay circuit 312 is conventional and suitable delay circuits can be implemented using conventional designs and circuitry well known by those ordinarily skilled in the art. In response to the SELBG signal being low, the multiplexer 310 outputs the VBG1 voltage as the VBG voltage applied to the charge pump 306. In contrast, when the SELBG signal is high, the multiplexer 310 outputs the VBG2 voltage as the VBG voltage applied to the charge pump 306. In one embodiment, the voltages VBG1 and VBG2 are equal. However, it will be appreciated that changes to the reference voltages VBG1 and VBG2 generated by the active and standby bandgap voltage references 302, 304, respectively, can be unequal as well without departing from the scope of the present invention.

Please amend the paragraph at page 7, line 22-page 8, line 12, as follows:

In operation, the bandgap switching circuit 300 operates in an active mode and a standby mode in response to the CEI# signal being active low and inactive high, respectively.

The active and standby modes of the bandgap switching circuit 300 correspond to the active and standby modes of operation of the flash memory containing the bandgap switching circuit. For the following description of the overall operation of the bandgap switching circuit 300, assume the band gap switching circuit 300 is initially operating in the active mode, with the CEI# and SELBG signals being low. In response to the low CEI# signal, the switch 314 applies the supply voltage VCC to the active bandgap voltage reference 302 which, in turn, generates the VBG1 voltage. The low SELBG signal also causes the multiplexer 310 to apply the VBG1 voltage to the charge pump 306 as the VBG voltage. The charge pump 306 thereafter operates as previously described to generate the VX voltage using the applied VBG voltage, and applies the VX voltage to the row drivers 308 which operate as previously described to selectively apply the VX voltage on the word lines WL1-WLN responsive to the decoded row address signals DRA1-DRAN. Note that during the active mode, the standby band gap voltage reference 304 generates the VBG2 voltage although this voltage is not utilized (the multiplexer 310 isolates this voltage). The standby bandgap voltage reference 304 consumes a relatively small amount of power, however, as previously mentioned, and thus does not significantly increase the power consumption of the flash memory during the active mode.

Please amend the paragraph at page 8, line 27-page 9, line 20, as follows:

When the CEI# signal goes low, the bandgap switching circuit 300 terminates operation in the standby mode and commences operation in the active mode. In response to the low CEI# signal, the switch 314 applies the supply voltage VCC to the active bandgap voltage reference 302 which, in turn, begins charging the VBG1 voltage to its desired value. At this point, although the CEI# signal is active low, the delay circuit 312 continues driving the SELBG signal high and thus the multiplexer 310 continues providing the VBG voltage from the standby bandgap voltage reference 304 to the charge pump 306. Recall, the delay circuit 312 does not drive the SELBG signal low until the delay time TD after the CEI# signal goes low. Thus, while the active bandgap voltage reference 302 is charging the VBG1 voltage to the desired value during the delay time TD, the standby bandgap voltage reference 304 supplies the VBG voltage to the charge pump 306. The charge pump 306 thus continues generating the VX voltage using

the VBG voltage from the standby bandgap voltage reference 304, allowing any of the row drivers 308 to activate the corresponding word line WL1-WLN using the VX voltage of the charge pump. As a result, if a data transfer command such as a read command is applied to the flash memory before expiration of the delay time TD, the selected row driver 308 can activate the corresponding word line WL1-WLN to access the addressed row of memory cells 100 (Figure 1). This is true even though the active bandgap voltage reference 302 has not yet charged the VBG1 voltage to the desired value. After expiration of the delay time TD, the delay circuit 312 drives the SELBG signal low causing the multiplexer 310 to apply the VBG voltage from the active bandgap voltage reference 302 to the charge pump 306 which thereafter operates as previously described in generating about VX voltage from the applied VBG voltage.

Please amend the paragraph at page 8, line 27-page 9, line 20, as follows:

When the CEI# signal goes low, the bandgap switching circuit 300 terminates operation in the standby mode and commences operation in the active mode. In response to the low CEI# signal, the switch 314 applies the supply voltage VCC to the active bandgap voltage reference 302 which, in turn, begins charging the VBG1 voltage to its desired value. At this point, although the CEI# signal is active low, the delay circuit 312 continues driving the SELBG signal high and thus the multiplexer 310 continues providing the VBG voltage from the standby bandgap voltage reference 304 to the charge pump 306. Recall, the delay circuit 312 does not drive the SELBG signal low until the delay time TD after the CEI# signal goes low. Thus, while the active bandgap voltage reference 302 is charging the VBG1 voltage to the desired value during the delay time TD, the standby bandgap voltage reference 304 supplies the VBG voltage to the charge pump 306. The charge pump 306 thus continues generating the VX voltage using the VBG voltage from the standby bandgap voltage reference 304, allowing any of the row drivers 308 to activate the corresponding word line WL1-N using the VX voltage of the charge pump. As a result, if a data transfer command such as a read command is applied to the flash memory before expiration of the delay time TD, the selected row driver 308 can activate the corresponding word line WL1-N to access the addressed row of memory cells 100 (Figure 1). This is true even though the active bandgap voltage reference 302 has not yet charged the VBG1

voltage to the desired value. After expiration of the delay time TD, the delay circuit 312 drives the SELBG signal low causing the multiplexer 310 to apply the VBG voltage from the active bandgap voltage reference 302 to the charge pump 306 which thereafter operates as previously described in generating about VX voltage from the applied VBG voltage. It will be appreciated by those ordinarily skilled in the art that the delay time TD can be equal to or greater than the time for the active bandgap voltage reference 302 to charge to the VBG1 voltage. However, as will be further appreciated, the particular length of the delay time TD can be modified without departing from the scope of the present invention.

Please amend the paragraph at page 10, line 19-page 11, line 3, as follows:

The bandgap switching circuit 300 utilizes the dual bandgap voltage references 302, 304 to reduce the power consumption of the flash memory containing the bandgap switching circuit, while at the same time keeping the transition time of the flash memory from the standby mode to the active mode relatively small. The power consumption is reduced by deactivating the relatively high power and high precision active bandgap voltage reference 302 during the standby mode and using the relatively low power standby bandgap voltage reference 304. In this way, the charge pump 306 utilizes the VBG2 voltage generated by the low power standby voltage reference 304 to maintain the VX voltage during the standby mode and the high power active voltage reference 302 is turned OFF. The less accurate VBG2 voltage can be used during the standby mode since the actual value of the VX voltage the charge pump 306 generates using the VBG2 voltage is less critical because the row drivers 308 are not actually applying the VX voltage to word lines WL1-WLN to access rows of memory cells 100 (Figure 1).

Please amend the paragraph at page 11, lines 4-18, as follows:

The bandgap switching circuit 300 reduces the transition time of the corresponding flash memory from the standby to active mode through the use of the dual voltage references 302, 304. The standby bandgap voltage reference 304 generates the VBG2 voltage while the active bandgap voltage reference 302 is charging the VBG1 voltage. In this way, a processor or other device can apply data transfer commands to the flash memory relatively

quickly after the memory is placed in the active mode, and the processor need not wait the relatively long time (200-300 nanoseconds as mentioned above) it takes the VBG1 voltage to charge to its required value. Note that during the active mode, the standby band gap voltage reference 304 generates the VBG2 voltage although the voltage is not being utilized. The standby bandgap voltage reference 304 consumes a relatively small amount of power, however, and thus does not significantly increase the power consumption of the flash memory during the active mode. One skilled in the art will understand various circuits that can be used in forming the components 302-314 in the bandgap switching circuit 300 of Figure 3A, and thus such circuits will not be described in detail herein.

Please amend the paragraph at page 12, lines 1-25, as follows:

Figure 4 is a functional block diagram of a flash memory 400 including the bandgap switching circuit 300 of Figure 3A. The bandgap switching circuit 300 is shown contained in a program/erase charge pump voltage switch 464, although the row drivers 308 (Figure 3A) would typically be contained in address decoders 440a, 440b, as will be appreciated by those skilled in the art. The operation of the program/erase charge pump voltage switch 464 and address decoders 440a, 440b will be discussed in more detail below. The flash memory 400 includes a command state machine (CSM) 404 that receives control signals including a reset/power-down signal RP#, a chip enable signal CE#, a write enable signal WE#, and an output enable signal OE#, where the "#" denotes a signal as being low true. An external processor (not shown) applies command codes on a data bus DQ0-DQ15 and these command codes are applied through a data input buffer 416 to the CSM 404. A command being applied to the flash memory 400 includes the control signals RP#, CE#, WE#, and OE# in combination with the command codes applied on the data bus DQ0-DQ15. The CSM 404 decodes the commands and acts as an interface between the external processor and an internal write state machine (WSM) 408. When a specific command is issued to the CSM 404, internal command signals are provided to the WSM 408, which in turn, executes the appropriate process to generate the necessary timing signals to control the memory device 400 internally and accomplish the requested operation. In response to the RP# and/or CE# signals, the CSM 404 develops applies

signals to the delay circuit 312 and switch 314 (see Figure 3A) to control the mode of operation of the bandgap switching circuit 300. In one embodiment, when the CE# signal goes active low, the CSM 404 drives the CEI# signal low, placing the bandgap switching circuit 300 in the active mode of operation. When the CE# signal goes inactive high, the CSM 404 drives the CEI# signal inactive high, placing the bandgap switching circuit 300 in the standby mode of operation.

Please amend the paragraphs at page 14, line 11-page 15, line 3, as follows:

The flash memory 400 operates in a standby power-savings mode when the RP# and CE# signals are both high, and operates in a reset deep power-down mode when the RP# signal goes active low. In response to the high CE# signal, the CSM 404 applies a high CEI# signal (Figure 3A) to the bandgap switching circuit 300 which, in turn, turns OFF the active bandgap voltage reference 302 (Figure 3A) as previously described, reducing the power consumption of the flash memory 400.

It will be appreciated that the embodiment of the flash memory 400 illustrated in Figure 5 has been provided by way of example and that the present invention is not limited thereto. Those of ordinary skill in the art have sufficient understanding to modify the previously described flash memory embodiment to implement other embodiments of the present invention. For example, although the bandgap switching circuit 300 is shown as being contained in the program/erase charge pump voltage switch 464 and the row decoders 308 (Figure 3A) indicated as being contained in the address decoders 440a, 440b, components of the bandgap switching circuit may be incorporated in other circuit blocks in the flash memory 400. The particular arrangement of the bandgap switching circuit 300 is a matter of design preference. Moreover, although the bandgap switching circuit 300 is described as including the bandgap voltage references 302, 304, other types of voltage reference circuits can also be utilized, as will be understood by those skilled in the art. Although the bandgap switching circuit 300 has been described with reference to flash memories, the circuit and principles described herein may also be applied to other types of memories and integrated circuits.